IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
	:	Group Art Unit: 1753
Robert Sheffield et al.	:	
	:	Examiner: Luan V. Van
Appln. No.: 10/667,491	:	
	:	Confirmation No.: 1242
Filed: September 23, 2003	:	
	:	Customer No.: 21967
For: REDUCED CIRCUIT TRACE ROUGHNESS FOR IMPROVED SIGNAL PERFORMANCE	:	

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AMENDED APPEAL BRIEF

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed May 24, 2006, and in response to the Notice of Panel Decision from Pre-Appeal Brief Review dated July 6, 2006.

REAL PARTY IN INTEREST

The Appellants, Robert Sheffield and Eileen Goulet, are the Applicants in the above-identified patent application. The Appellants have assigned their entire interest in the above-identified patent application to Nortel Networks Limited, 2351 Boulevard Alfred-Nobel, St. Laurent, Quebec, H4S 2A9 Canada.

RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' legal representative, and the Assignee are not aware of any other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this Appeal.

STATUS OF CLAIMS

Claims 1-20 are pending in the above-identified patent application. Claims 7-18 were withdrawn from consideration by the Examiner in an Office Action dated October, 19, 2005. Claims 1-6, 19, and 20 were finally rejected in an Office Action dated March 8, 2006. The final rejection of Claims 1-6, 19, and 20 is hereby appealed.

Claims 1-6, 19, and 20 stand rejected under 35 U.S.C. § 102(b), as either being anticipated by or obvious in view of Tanaka et al. (U.S. Patent No. 4,959,507), Taylor et al. (U.S. Patent No. 6,309,528), Ozeki et al. (U.S. Patent Application Publication No. US2002/0060090), Nagai et al. (U.S. Patent Application Publication No. US2002/0155021), Taylor et al. (U.S. Patent No. 6,558,231), and Lin et al. (U.S. Patent No. 5,273,938).

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection of claims 1-6, 19, and 20 in the Office Action dated March 8, 2006.

SUMMARY OF THE CLAIMED INVENTION

The claimed invention, as set forth in claim 1, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, is directed to a method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board (e.g., see Figure 3; page 13, line 3, to page 16, line 1). The method may comprise providing a layer of the circuit board having the conductive circuit trace on a surface thereof (e.g., see Figure 3; page 13, lines 8-17). The method may also comprise reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace (e.g., see Figure 3; page 13, line 18, to page 15, line 20).

The claimed invention, as set forth in claim 2, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be

further defined by the step of reducing the surface roughness including one of a group consisting of: electropolishing the at least one surface; chemical polishing the at least one surface; electrochemical polishing the at least one surface; chemical-mechanical polishing the at least one surface; mechanical polishing the at least one surface; electroplating the at least one surface; and vacuum depositing conductive material on the at least one surface (e.g., see Figure 3; page 13, line 18, to page 15, line 20).

The claimed invention, as set forth in claim 3, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the surface roughness of the at least one surface being reduced to no more than 20 microinches root-mean-squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 4, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the surface roughness of the at least one surface being reduced to no more than 10 microinches root-mean-squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 5, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the surface roughness of the at least one surface being reduced to no more than 5 microinches root-mean-squared (RMS) (e.g., see Figure 3; page 9, line 18, to page 10, line 4).

The claimed invention, as set forth in claim 6, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the at least one surface of the conductive circuit trace including one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board (e.g., see Figure 3; page 11, line 18, to page 12, line 21).

The claimed invention, as set forth in claim 19, and as described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the conductive circuit trace being formed on the surface of the circuit board layer (e.g., see Figure 3; page 13, lines 8-10).

The claimed invention, as set forth in claim 20, and as

described and shown in the specification and Figures 1A-3 of the above-identified patent application, respectively, may be further defined by the conductive circuit trace being affixed to the surface of the circuit board layer (e.g., see Figure 3; page 13, lines 8-10).

GROUNDS OF REJECTION ON APPEAL

Claims 1-6, 19, and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 4,959,507).

Claims 1, 2, 6, and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by either Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090).

Claims 3-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Nagai et al. (U.S. Patent Application No. 2002/0155021) or Taylor et al. (U.S. Patent No. 6,558,231).

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Lin et al. (U.S. Patent No. 5,273,938).

ARGUMENT

The Appellants respectfully appeal the decision of the Examiner to finally reject claims 1-6, 19, and 20 of the above-identified patent application. As discussed below, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation or obviousness against the appealed claims.

I. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIMS 1-6, 19, AND 20

The Examiner asserts that claims 1-6, 19, and 20 are anticipated by Tanaka et al. (U.S. Patent No. 4,959,507) under 35 U.S.C. § 102(b).

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the

claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 1, the Examiner asserts that Tanaka et al. teaches the claimed invention. Applicants respectfully disagree for several reasons. Specifically, the Examiner implies that Tanaka et al. teaches a method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board as set forth in claim 1. However, as acknowledged by the Examiner, Tanaka et al. teaches a method for forming a bonded ceramic-metal composite substrate. Thus, the teaching of Tanaka et al. clearly differs from the claimed method as set forth in claim 1.

Also, the Examiner asserts that Tanaka et al. teaches reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. However, Tanaka et al. fails to teach, or even suggest, improving the performance of a signal transmitted via a conductive circuit trace by

reducing a surface roughness of at least one surface of the conductive circuit trace, as claimed. Indeed, Tanaka et al. fails to teach, or even suggest, anything regarding polishing a copper circuit sheet so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. Instead, Tanaka et al. teaches polishing a copper circuit sheet so as to improve heat transmissivity between the copper circuit sheet and an electronic component (e.g., see from column 3, line 64, to column 4, line 13). Indeed, Tanaka et al. even teaches that polishing is only required where an electronic component is to be mounted to a copper circuit sheet so as to improve heat transmissivity therebetween, and that polishing is not required where the electronic component is electrically connected to copper circuit sheet, which would be where signals are transmitted (e.g., see from column 1, line 67, to column 2, line 7; column 3, lines 1-8). Such a teaching by Tanaka et al. is not even analogous to the claimed invention. Thus, since the method taught by Tanaka et al. is totally different and non-analogous to the claimed invention, Applicants respectfully submit that Tanaka et al. fails to teach, or even suggest, the claimed invention.

In view of the foregoing, it is respectfully submitted that Tanaka et al. fails to teach, or even suggest, the claimed

invention as set forth in claim 1. Thus, is it further respectfully submitted that claim 1 is allowable over Tanaka et al..

Claims 2-6, 19, and 20 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka et al. fails to disclose any of these claimed techniques. Also, claims 3-5 recite that the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS), 10 microinches root-mean-squared (RMS), or 5 microinches root-mean-squared (RMS). The Examiner asserts that Tanaka et al. teaches such surface roughnesses by disclosing a mounting area median surface roughness no greater than 3 μm and a mounting area maximum surface roughness no greater than 18 μm. However, 20 microinches translates into

.508 μm, 10 microinches translates into .254 μm, and 5 microinches translates into .127 μm. Clearly, the claimed surface roughnesses are well below the 3 μm median surface roughness set by Tanaka et al., and they are not associated with a mounting area. Accordingly, Tanaka et al. fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka et al. fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully submitted that Tanaka et al. fails to disclose, or even suggest, the elements of claims 1-6, 19, and 20. Accordingly, it is respectfully submitted that claims 1-6, 19, and 20 of the present application are not anticipated by Tanaka et al., and thus the Examiner has failed in his duty to establish at least a prima facie case of anticipation against claims 1-6, 19, and 20 of the present application. Therefore, it is respectfully requested that the anticipation rejection of claims 1-6, 19, and 20 be withdrawn.

II. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIMS 1, 2, 6, AND 19

The Examiner asserts that claims 1, 2, 6, and 19 are anticipated by either Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) under 35 U.S.C. § 102(b).

Regarding claim 1, the Examiner asserts that both Taylor et al. and Ozeki et al. teach methods for electroplating on at least one surface of a conductive circuit trace. However, it is respectfully submitted that neither Taylor et al. nor Ozeki et al. teach providing a layer of a circuit board having a conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. In contrast, Taylor et al. merely discloses a method of depositing metallic conductors onto the surface of circuit boards, wherein conductive metal is deposited to accommodate both small and large features, while Ozeki et al. merely discloses a method for manufacturing a printed circuit board having a shielded transmission line in order to reduce the effects of external noise. Thus, it is respectfully submitted that neither Taylor et al. nor Ozeki et al. disclose, or even suggest, providing a layer of a circuit board having a

conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. Accordingly, it is respectfully submitted that claim 1 should be allowable over Taylor et al. and Ozeki et al..

At this point it should be noted that if the Examiner is going to rely upon the theory that the claimed invention is inherent in either Taylor et al. or Ozeki et al., "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Claims 2, 6, and 19 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2, 6, and 19 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, as

discussed above, these claims recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that Taylor et al. and Ozeki et al. both fail to disclose, or even suggest, the elements of claims 1, 2, 6, and 19. Accordingly, it is respectfully submitted that claims 1, 2, 6, and 19 of the present application are not anticipated by either Taylor et al. or Ozeki et al., and thus the Examiner has failed in his duty to establish at least a prima facie case of anticipation against claims 1, 2, 6, and 19 of the present application. Therefore, it is respectfully requested that the anticipation rejection of claims 1, 2, 6, and 19 be withdrawn.

III. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF OBVIOUSNESS AGAINST CLAIMS 3-5

The Examiner asserts that claims 3-5 are unpatentable over Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Nagai et al. (U.S. Patent Application No. 2002/0155021) or Taylor et al. (U.S. Patent No. 6,558,231) under 35 U.S.C. § 103(a).

It is respectfully submitted that the obviousness rejection of claims 3-5 has become moot in view of the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed

above with respect to independent claim 1. That is, claims 3-5 are dependent upon independent claim 1 and thus inherently incorporate all of the limitations of independent claim 1. Also, secondary references Nagai et al. and Taylor et al. fail to disclose, or even suggest, the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed above with respect to independent claim 1. Indeed, the Examiner does not even assert such. Thus, the combination of secondary references Nagai et al. and Taylor et al. with the primary references Taylor et al. and Ozeki et al. also fails to disclose, or even suggest, the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed above with respect to independent claim 1. Accordingly, claims 3-5 should be allowable over the combination of the secondary references Nagai et al. and Taylor et al. with the primary references Taylor et al. and Ozeki et al. at least by virtue of their dependency on independent claim 1. Moreover, as discussed above, claims 3-5 recite additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that the combination of the primary references Taylor et al. and Ozeki et al. with the secondary references Nagai et al. and

Taylor et al. fails to disclose, or even suggest, the elements of claims 3-5. Accordingly, it is respectfully submitted that claims 3-5 of the present application are not unpatentable over the combination of the primary references Taylor et al. and Ozeki et al. with the secondary references Nagai et al. and Taylor et al., and thus the Examiner has failed in his duty to establish at least a prima facie case of obviousness against claims 3-5 of the present application. Therefore, it is respectfully requested that the obviousness rejection of claims 3-5 be withdrawn.

IV. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF OBVIOUSNESS AGAINST CLAIM 20

The Examiner asserts that claim 20 is unpatentable over Taylor et al. (U.S. Patent No. 6,309,528) or Ozeki et al. (U.S. Patent Application No. 2002/0060090) in view of Lin et al. (U.S. Patent No. 5,273,938) under 35 U.S.C. § 103(a).

It is respectfully submitted that the obviousness rejection of claim 20 has become moot in view of the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed above with respect to independent claim 1. That is, claim 20 is dependent upon independent claim 1 and thus inherently incorporates all of the limitations of independent claim 1. Also, secondary reference Lin et al. fails to disclose, or even

suggest, the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed above with respect to independent claim 1. Indeed, the Examiner does not even assert such. Thus, the combination of secondary reference Lin et al. with the primary references Taylor et al. and Ozeki et al. also fails to disclose, or even suggest, the deficiencies of the primary references Taylor et al. and Ozeki et al. as discussed above with respect to independent claim 1. Accordingly, claim 20 should be allowable over the combination of the secondary reference Lin et al. with the primary references Taylor et al. and Ozeki et al. at least by virtue of their dependency on independent claim 1. Moreover, claim 20 recites additional features which are not disclosed, or even suggested, by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully submitted that the combination of the primary references Taylor et al. and Ozeki et al. with the secondary reference Lin et al. fails to disclose, or even suggest, the elements of claim 20. Accordingly, it is respectfully submitted that claim 20 of the present application is not unpatentable over the combination of the primary references Taylor et al. and Ozeki et al. with the secondary reference Lin et al., and thus the Examiner has failed in his duty to establish at least a prima facie case of

obviousness against claim 20 of the present application. Therefore, it is respectfully requested that the obviousness rejection of claim 20 be withdrawn.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation or obviousness against the appealed claims. Thus, it is respectfully submitted that the final rejection of claims 1-6, 19, and 20 is improper and the reversal of same is clearly in order and respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made.

Please note that the fee of $500.00 for the Appeal Brief filing was already paid on August 7, 2006. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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CLAIMS APPENDIX

1 (Previously Presented). A method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board, the method comprising the step of:

providing a layer of the circuit board having the conductive circuit trace on a surface thereof; and

reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace.

2 (Previously Presented). The method as in Claim 1, wherein the step of reducing the surface roughness includes one of a group consisting of: electropolishing the at least one surface; chemical polishing the at least one surface; electrochemical polishing the at least one surface; chemical-mechanical polishing the at least one surface; mechanical polishing the at least one surface; electroplating the at least one surface; and vacuum depositing conductive material on the at least one surface.

3 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than

20 microinches root-mean-squared (RMS).

4 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 10 microinches root-mean-squared (RMS).

5 (Original). The method as in Claim 1, wherein the surface roughness of the at least one surface is reduced to no more than 5 microinches root-mean-squared (RMS).

6 (Original). The method as in Claim 1, wherein the at least one surface of the conductive circuit trace includes one of a group consisting of: a surface parallel and distal to a surface of the circuit board; a surface parallel and proximal to the surface of the circuit board; and a surface perpendicular to the surface of the circuit board.

7-18 (Withdrawn).

19 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is formed on the surface of the circuit board layer.

20 (Previously Presented). The method as in Claim 1, wherein the conductive circuit trace is affixed to the surface of the circuit board layer.

EVIDENCE APPENDIX

[NONE]

RELATED PLEADINGS APPENDIX

[NONE]